Earth Science Technology Conference 2003

Radiation Tolerant Ultra Low Power CMOS Microelectronics: Technology Development Status

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CONTENT

- Technology Background
- Performance
- Potential Impact on S/C and Science
- Future Work

Radiation Tolerant and Radiation Hard

Radiation Hard

- 1Meg rads Total Dose
- No latchup
- SEU ~ 40 LET

Radiation Tolerance

- 100K rads Total Dose
- No latchup
- SEU ~ 40 LET

RT ULP

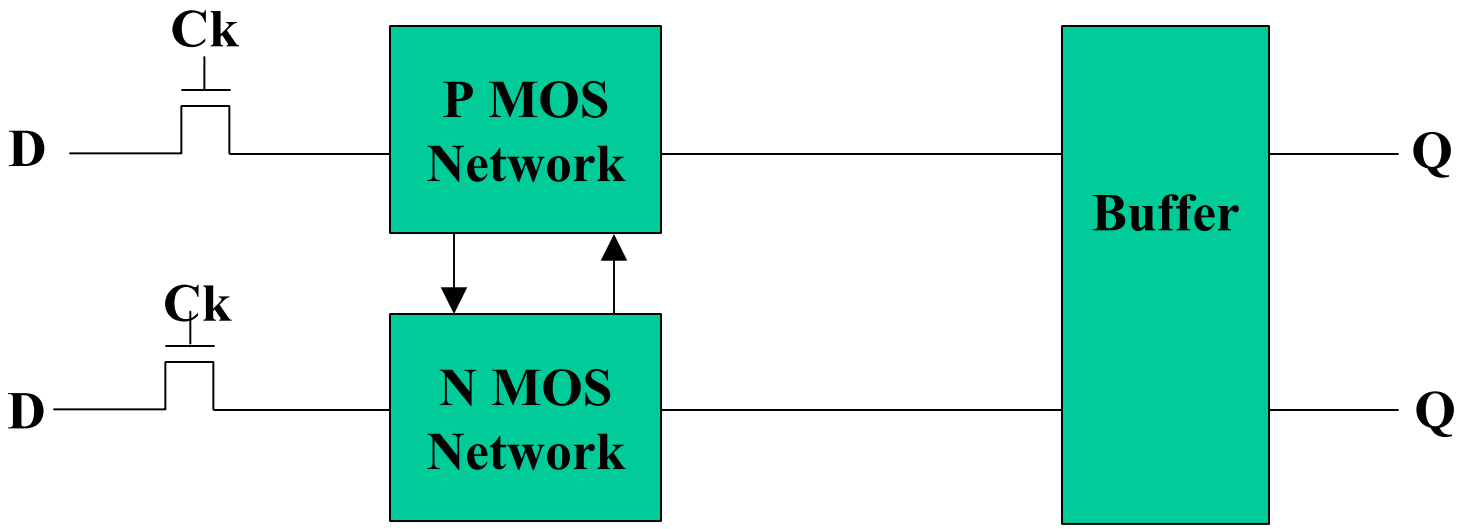
- ~ 1 Meg rad expected
- No latchup
- SEU ~ 40 LET
- Dose Rate designed

Radiation Tolerance

1. SEU tolerance by electrical design
2. Latchup through guard bar layout
3. Total dose through fabrication process*
4. Commercial foundry based

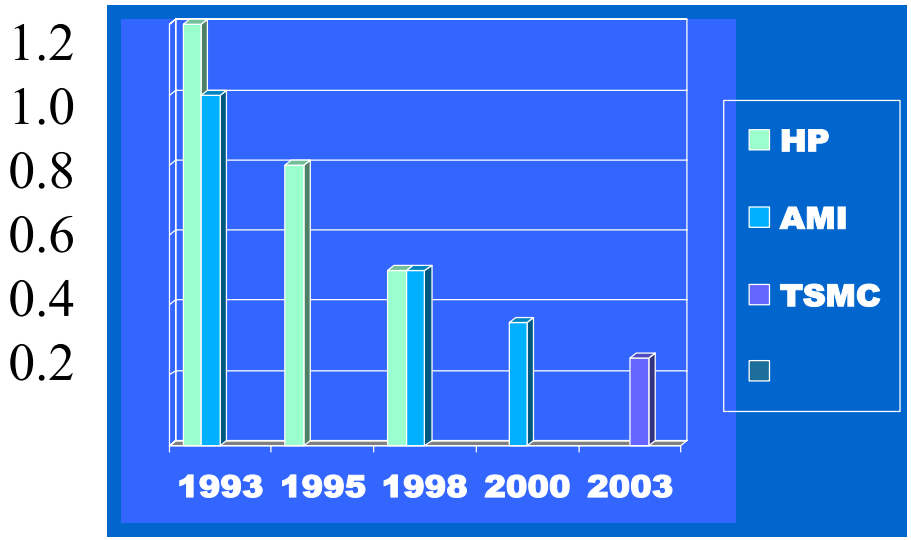
* Dramatic total dose increase through Ultra Low Power design

RT Overview

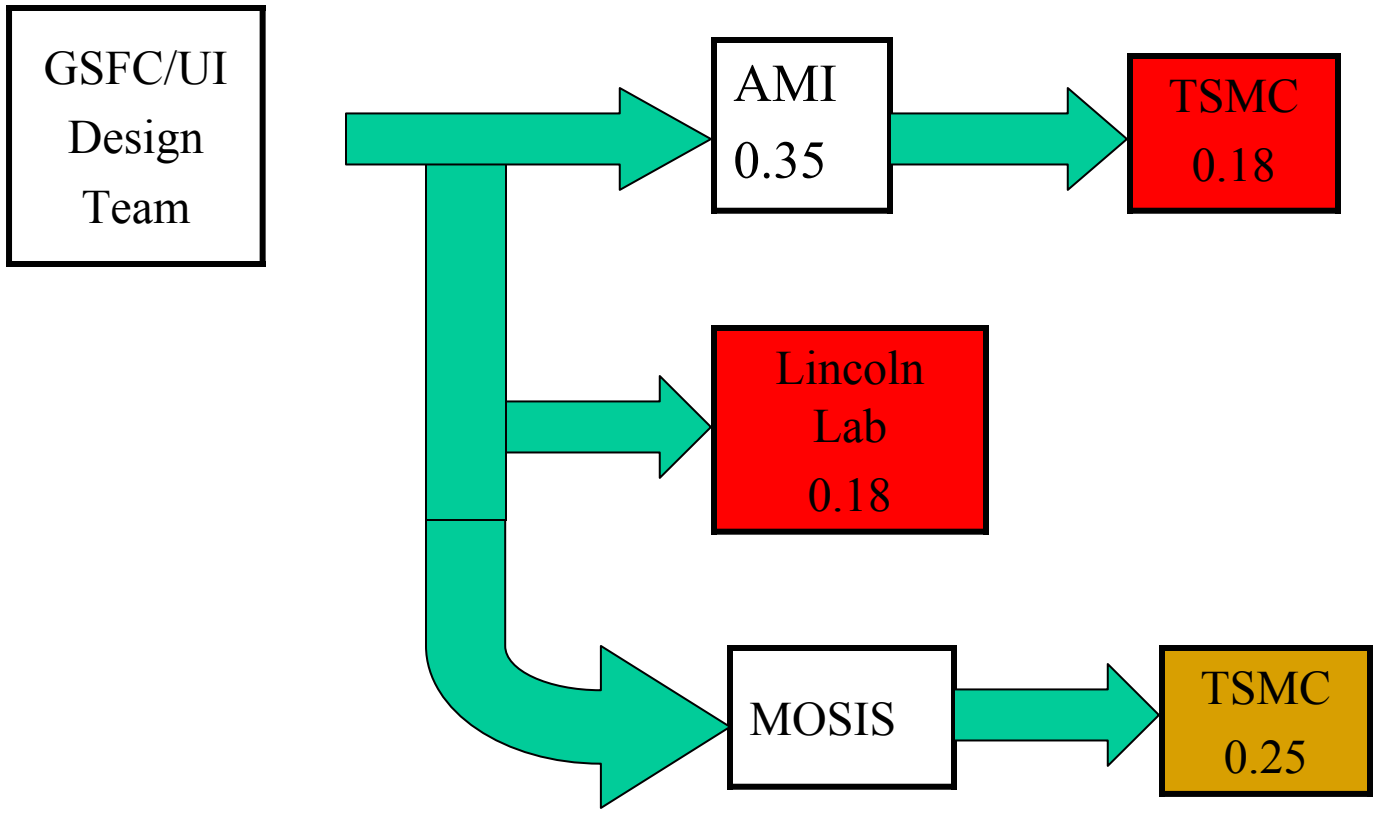


- Data stored in 2 networks
- Current flows in known direction when particle hits
- Feedback corrects faulty mode
- Incorrect state can not propagate

RT Process Experience

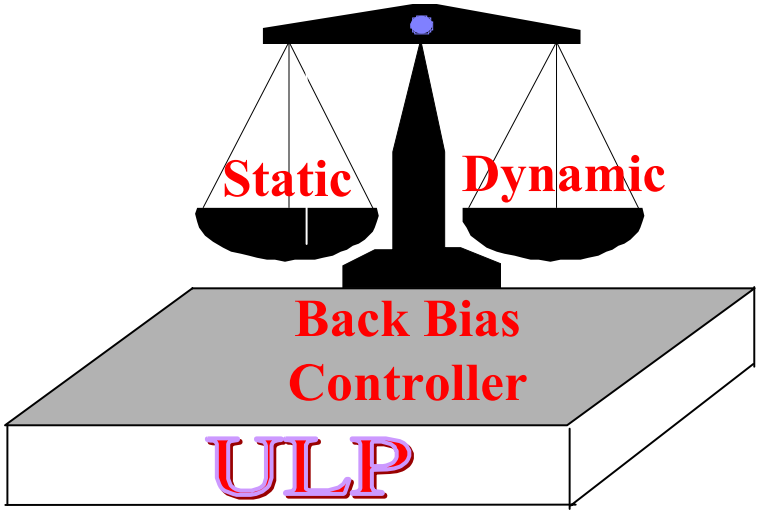


Available Foundries



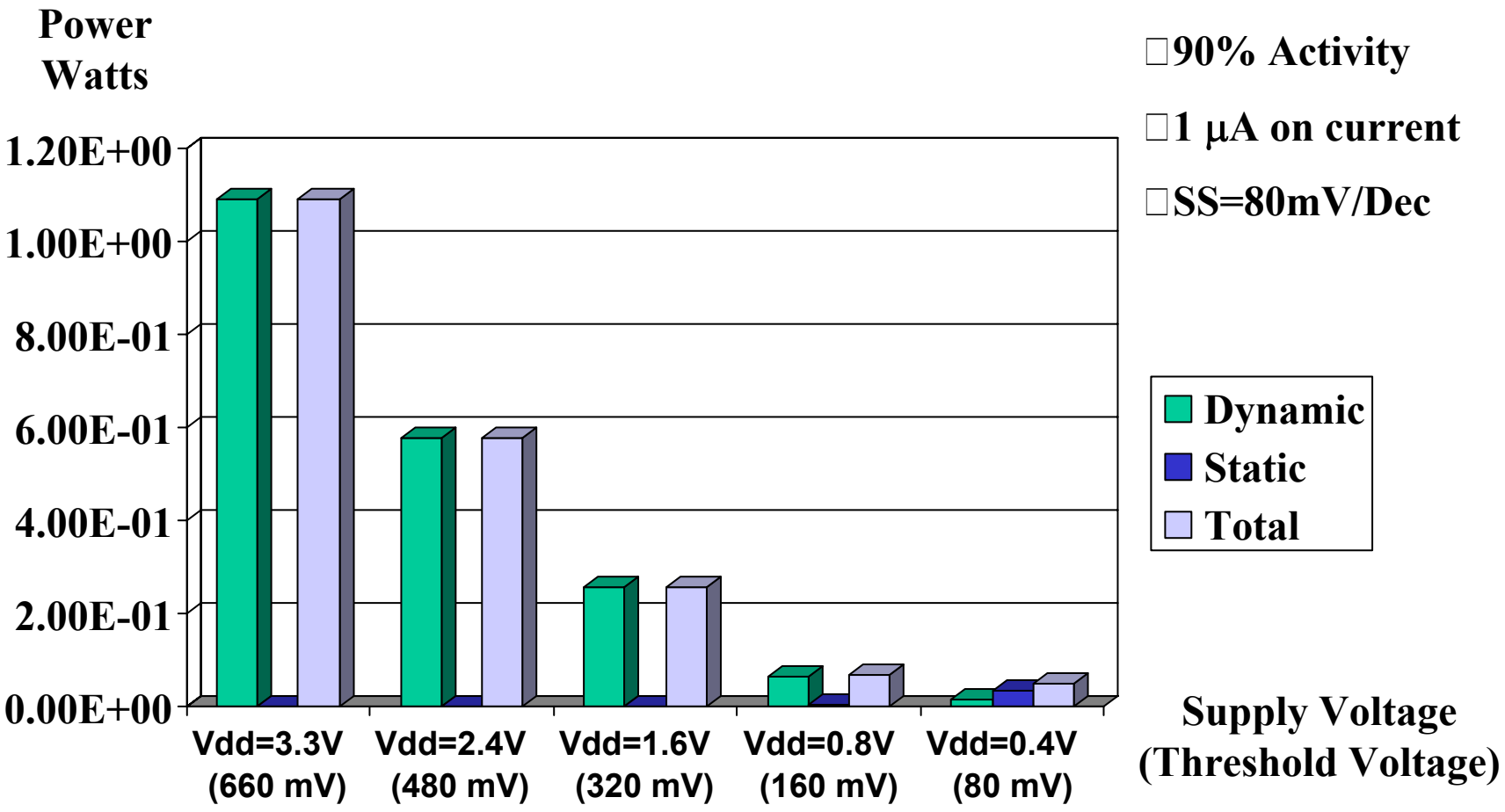
ULP Fundamentals

- Current CMOS Power (3.3V switching)
  - > 90% dynamic
  - < 10% static
- ULP (0.5V switching)
  - 50% dynamic
  - 50% static



- Results in 40:1 power reduction

1M Transistor Design
(Constant 5X Overdrive)



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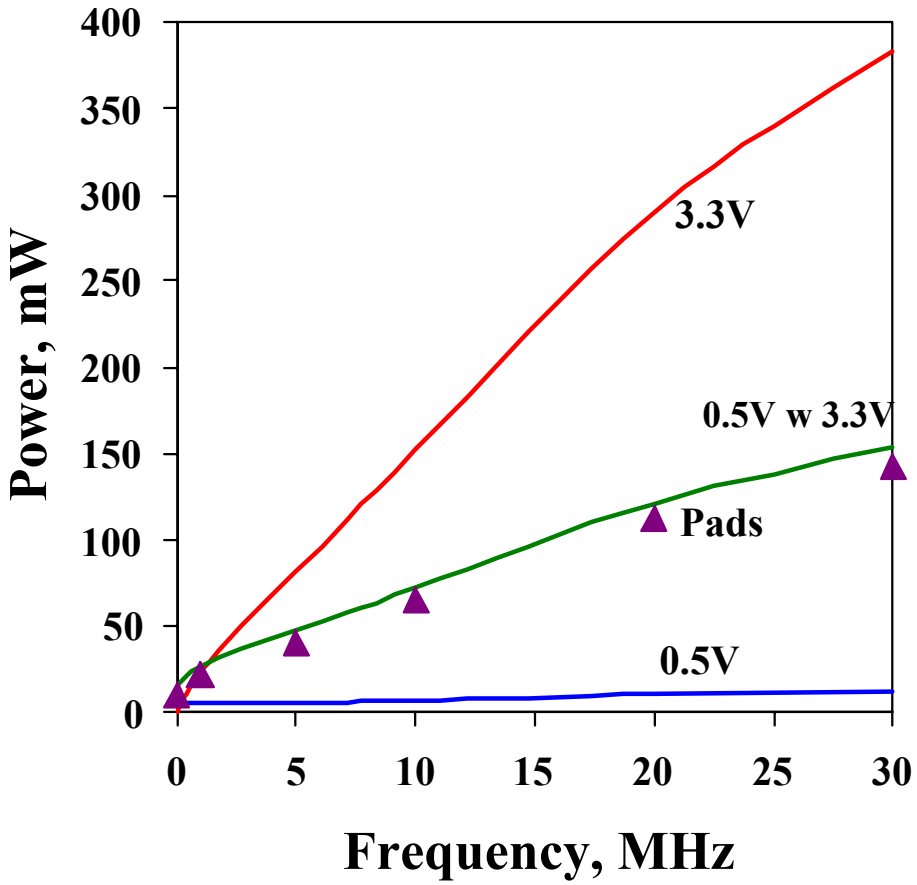
Power Comparisons



- Up to 30x savings in power for ULP part
- Power savings increases with frequency
  - Static power of ULP parts exceeds that of 3.3V part
  - More power consumed switching at high voltages
- Dynamic power of ULP with 3.3V pads is much less than 3.3V part. Power consumption dominated by pad power.

Area Impact

- Main Issue in "hardening by design" is providing protection for SEU events.
  - In FPGA, configuration logic dominates chip area. Triple Modular Redundancy (TMR) used in Xilinkx million gate FPGA. Recent work at LANL shows TMR version of a given design required 4X hardware ➔ resulting design more sensitive to SEUs than a non-redundant design.
  - RTULP technique has only 2X hardware impact.

ULP Chips

- CCSDS Lossless Data Compression Chip (RT ULP)
  - 450 Mbps @13 mwatts
- CCSDS R-S channel encoder (RT ULP)
  - 200 Mbps @ 4 mwatts ➔ tech demo on ST 5/NMP
- 8051 micro-controller (RT ULP)
- C50 DSP chip (ULP only)
- 500 Mhz correlator (RT ULP) for GSFC's radiometer (B3P4 by Principe, et al)
  - ECL design required ~ 20 watts.
  - Current RT ULP chip ~ 10 mwatts
- Cross correlator (RT ULP) (B3P4 by Principe, et al)
  - < 1 watt for 25 channels over 200 Msamples/s

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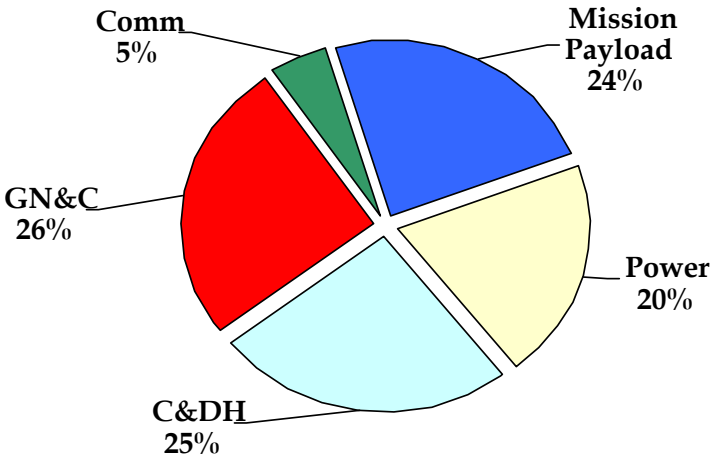
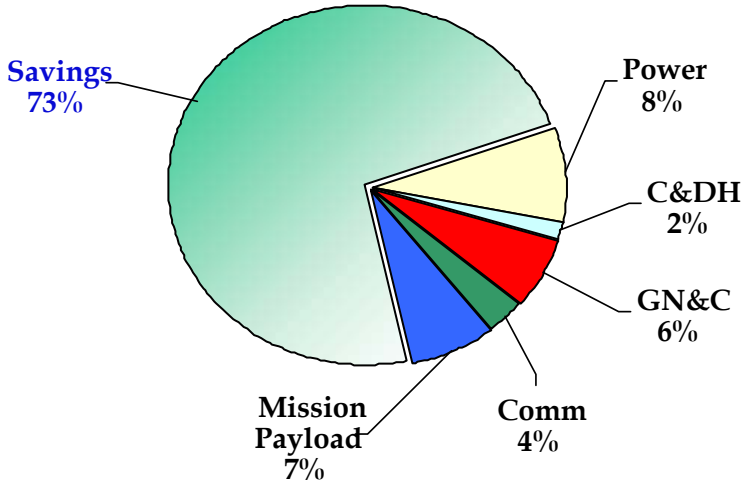
Re-engineering with ULP

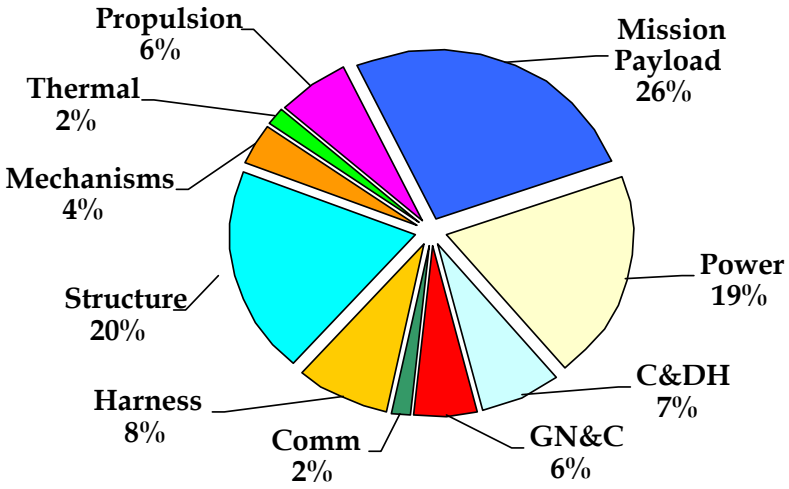
NMP EO-1 as Designed Power



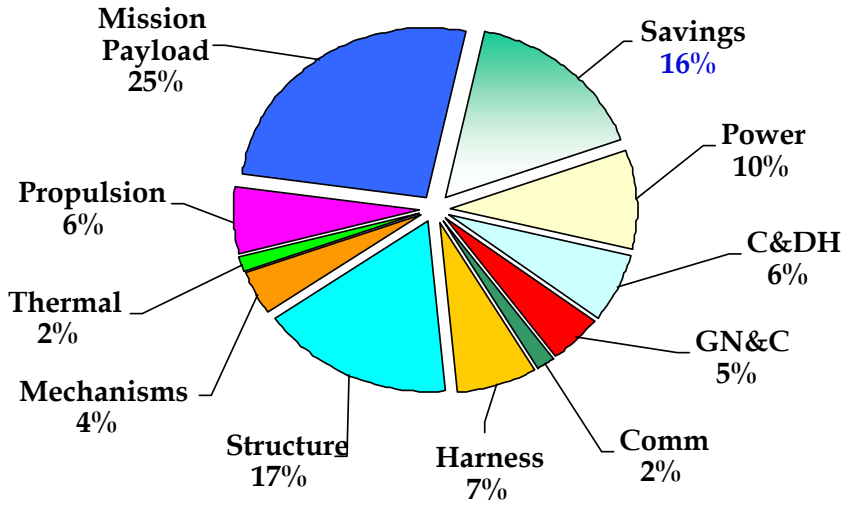
NMP EO-1 Power After ULP



NMP EO-1 as Designed Mass

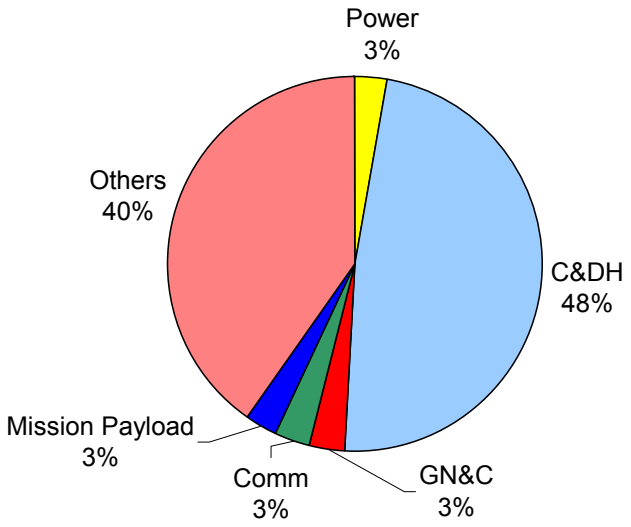


NMP EO-1 Mass After ULP

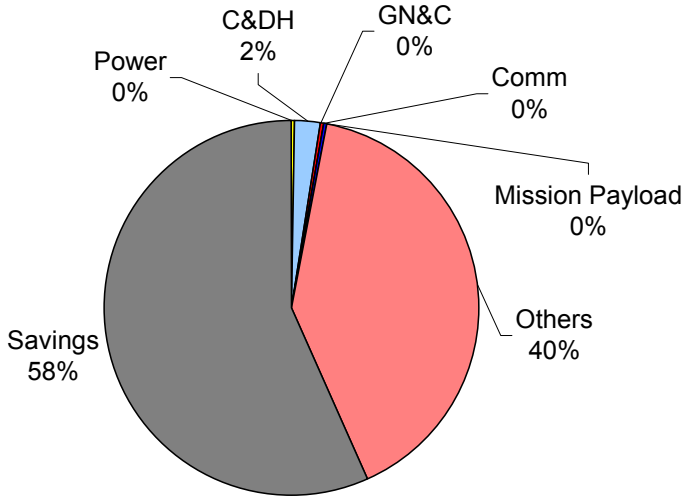


Potential Power Savings on ST5/NMP Using RT ULP

ST5 Power As Designed



ST5 Power After ULP

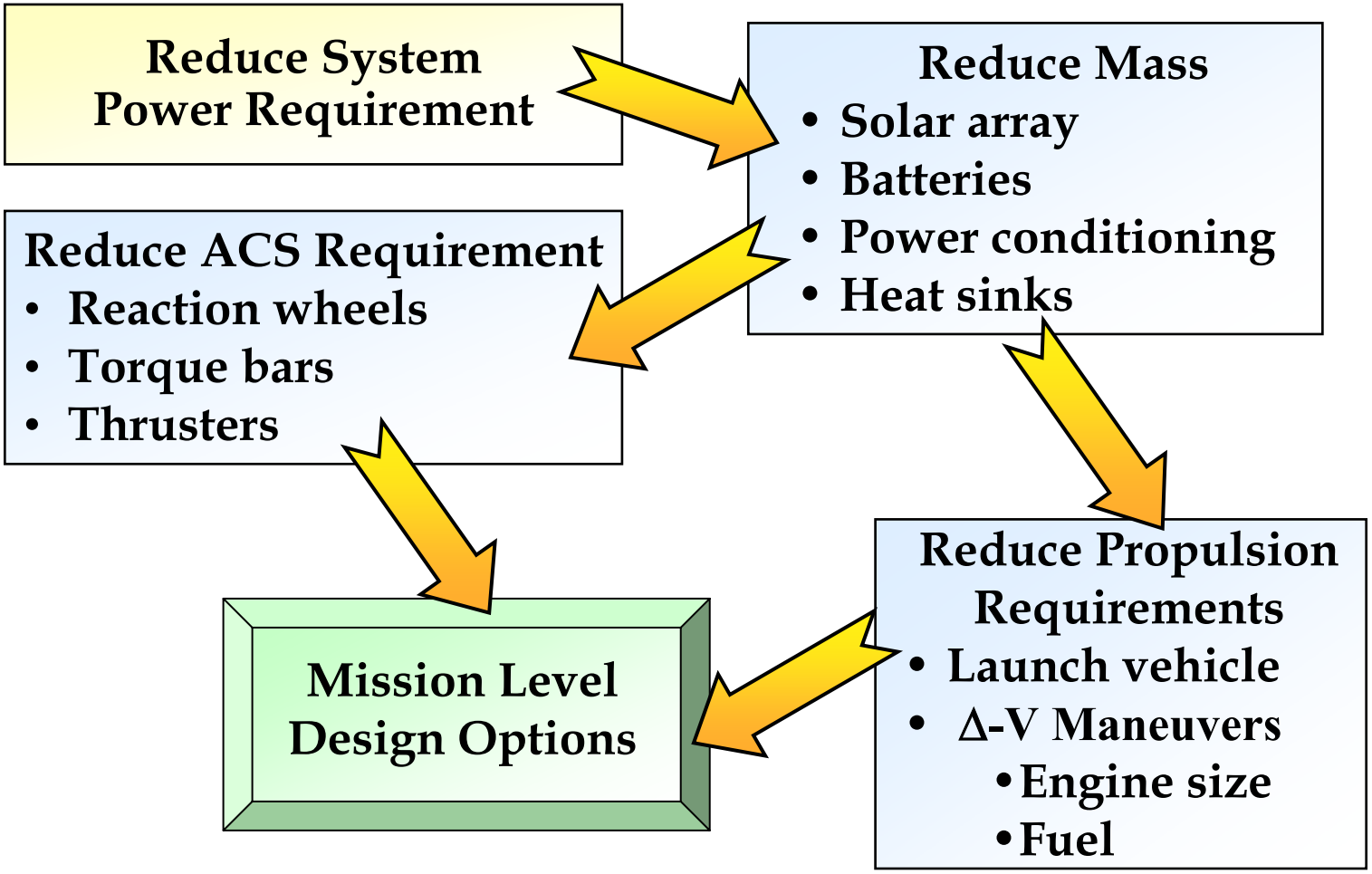


All analog power is included in “Others”

APL Study

- M. Freeman at APL/JPH, 1999 study report
  - Studied 5 missions:
    - Discover II: SAR
    - SLIC: passive sensors
    - FUSE: telescope, 1999
    - TIMED:Atmospheric Science, 2000
    - MSX: Sensor platform, 1996
  - Freeman's report: "We found load power reductions ranging from 20% to 41%, depending on the extent to which digital electronics are employed in the architecture."

The "Domino" Effect



Impact on Science

RT ULP enables NEW science instrument concept

=➔ New Discovery

e.g. Proposed Synthetic Thinned Aperture Radiometer (STAR) on GPM

Proposed STAR Instrument electronics: 2 channels with 25/19 receivers. Correlation for every pair of receivers.

- Projected correlator ASIC power > 40 watts
- Instrument electronics box limited to < 30 watts with control electronics, compression and H/K boards
- Projected RT ULP correlator power < 1 watt

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RT ULP Technology Features

- **Lower Power with 0.5 volt supply**
  - System level payoff studies on two missions
    - 50% spacecraft power reduction
    - 15% mass reduction realized from lower power
- **Performance Equivalent to 3.3 volt Commercial CMOS**
- **Commercial Foundry Based**
  - Higher performance with respect to radiation hard foundries
  - No cost to Government to support and upgrade foundry
  - Follow commercial road map to smaller feature sizes
  - Lower fabrication cost
- **Radiation Tolerant**
  - Latch-up Immune
  - SEU tolerant
  - Total dose tolerance projected to 1Mrad from back-bias

ULP Electronics

- 0.5 volt triple metal 0.35 micron CMOS process
  - Analog is coming up
  - Digital is quite solid, near completion
  - Four process runs completed at AMI
- Design Infrastructure
  - SPICE models (based on few runs)
  - Layout rules for RT and non-RT
  - Standard cell library in development
- 3.3 and 0.5 volt translation I/O pads

Future Work

- Complete RT ULP development for digital design –Automatic Back Bias generation
- Complete radiation test on devices from the ULP3 run
- Continue RT ULP work for analog/mixed signal
- Develop RT ULP components for S/C sub-systems
  - stable power supply converter and distribution components
  - DSP, general purpose processors, memory, ADC, protocol, etc.
- Research High Density design methodology to offset high mask cost for designs using features
- Develop mechanism for RT and ULP on smaller features: 0.25u and 0.18u
- Research Ultra Low Temperature potential capability